PERFORMANCE AND LIMITATIONS OF FETs AS MICROWAVE POWER AMPLIFIERS*

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Abstract

The GaAs FET has excellent potential as a microwave power amplifier and has demonstrated an f_t^2 (PX) product exceeding that of silicon bipolar devices. The design, fabrication, and performance limitations of GaAs power FETs is discussed. Experimental results for a multigate 4 GHz device and a single gate 7 GHz device are presented.

Introduction

This paper discusses the suitability of GaAs FETs as microwave power amplifiers, structures and technology used in these devices, and finally presents results obtained on experimental transistors.

GaAs vs. Si for High Power X-Band Transistors

Figure 1 shows the state-of-the-art of microwave power transistors for both silicon bipolar and GaAs FET devices. The data, following E.O. Johnson[1], is presented as square root of the power-output reactance product and is plotted versus f_t, the frequency at unity current gain. This form of normalization is particularly convenient to use since

$$\sqrt{(P_o X)} f_t = \frac{E_m v_s}{2\pi} \quad , \qquad (1)$$

where E_m and v_s are the avalanche electric field and saturation velocity respectively. The breakdown field of GaAs is 10% greater than that of silicon and the saturation velocity of GaAs is twice that of silicon. The power impedance of GaAs is 2.2 times that of silicon thus GaAs devices are potentially superior to silicon devices for power amplifiers. The open circle data points are CW measurements for state-of-the-art silicon bipolar transistors.[2] The solid circles are data points taken at 4 GHz, 7 GHz and 10 GHz on GaAs FETs. The 4 GHz data is for a multigate FET which delivered 0.8 watts, the 7 GHz data is for a single gate device delivering 0.1 watts. The last data point was one reported by Liechti at the 1972 ISSCC[3] for a single gate device delivering 0.03 watts. None of these power levels are excessively high, but when you consider them in the light of the per unit admittance, the GaAs data points are a factor of three higher than that of silicon and behave generally as predicted by Johnson.

Contact Resistance or Breakdown Voltage - A Compromise

Figure 2 shows some of the compromises that have to be made in designing a high power FET with GaAs. The requirements for high power operation of transistors call for large voltage as well as high current swings. High breakdown voltage Schottky-barrier gate electrodes on moderately high resistivity material having a density of the order of 2 to 4 x 10^{16} per cm^3 must be used to achieve high voltage capability. The requirement of high current density implies that low resistance contacts must be used and this is best accomplished with low resistivity material having a density of the order of 5×10^{18} per cm^3. The limitations inherent in GaAs technology preclude the use of low resistivity diffusions in n-type material to achieve low resistance contact areas in the high resistivity channel layers. For this reason, we have developed a technology based on a double layer epitaxy containing a low resistivity ohmic contact layer, and a moderately high resistivity Schottky-barrier contact layer.

Gate Width Consideration - A Multigate Design

In order to maximize the output power of a device, the source periphery must be made as large as possible. A large source periphery is accompanied by a correspondingly large gate width. Since the gate metalization has a finite resistance, and since the gate is on top of a depletion layer capacitance, the composite gate metalization and depletion layer takes the form of an R-C transmission line. A signal propagating on this line suffers an exponential decay. The practical limit on gate width occurs when the signal at one end of the gate is considerably lower than the signal at the input end. Therefore any further increase in gate width is not accompanied by corresponding increase in channel current modulation. In other words, part of the channel is being modulated, while another part is not. This is illustrated in curve of Fig. 3. The reduction in channel current modulation becomes significant when the gate widths equal the decay length. For 3000 Å evaporated gold of gate metalization, and for channel layer thickness of the order of 1/2 micron, the maximum gate width is 0.016". Further increases in device power must now be accompanied by an increase in the number of parallel units. Since all the contacts to the device are on the same side, paralleling of units requires at least one crossover. For example, if all the gates were interconnected on the surface of the substrate monolithically, and if all the drains were interconnected monolithically, a crossover would be necessary to interconnect all the sources. The parasitic capacity added by a crossover may be prohibitively large since the source electrode interconnects must cross over the drain metalizations with an oxide insulator providing the electrical separation between them. Therefore, paralleling must be accomplished by an alternate system.

Layout and Processing of a Multigate FET

The layout of the device shown in Fig. 4 is that of a multi-parallel-gate-structure with minimum crossover capacitance. There are 16 gates that are 3 to 4 microns long, and 0.016" wide. The gates are subdivided into pairs in the form of a "V", with the drain in the center of the "V", and the sources on the sides. The gate bonding pad joins the gates at the bottom of the "V". The sub-units are isolated since each drain electrode is common only to one gate electrode but adjacent sub-units have a common source electrode. Since the sub-units could be interconnected by bond wires there is no degradation due to overlay capacity.

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The active device size, 0.050" in the long dimension, is about as small as one can make it and still wire bond to each individual sub-unit. A smaller device size would have to be accompanied by an overlay interconnect technique but this overlay would have to be done without significantly increasing feedback or output capacity.

The cross-section in Fig. 4 illustrates the salient features of the device fabrication. An initial evaporation on the heavily doped n-plus layer forms the ohmic contact. A narrow gap is formed in the ohmic contact to form a source and drain and exposes the n-plus gallium arsenide over the channel region. A semiconductor etch is then used to remove the n-plus layer in the gap, and expose the relatively high resistivity layer. Finally, the gate electrode is formed by a second metal evaporation which condenses precisely between the source and drain without short circuiting because of the cantilever effect of the overhanging source and drain electrodes. The entire device is in the form of a mesa so that the gate bonding pad lies on the semiinsulating surface of the gallium arsenide, and therefore avoids that form of parasitic capacity. The region where the gate bonding pad connects to the gate electrode is shown in the scanning electron micrograph of Fig. 5. It is easy to see that the gate bonding pad on the lowest level, rides up the edge of the mesa, and covers the channel region as a Schottky-barrier gate electrode. The source and the drain electrodes are at yet a higher level than the channel region. Fig. 6 is a photo of the FET in the microstrip test fixture. The inset is a blowup of the multigate FET showing how it is bonded into the microstrip circuitry and illustrating the limiting case of close spaced bonding wires. Each individual gate pad is bonded to the input, and each drain pad to the output. All of the sources are grounded. The stubs that are evident on the microstrip line are gold-plated magnetic material, and are held in place by magnets on the bottom of the substrate. Tuning is accomplished by simply pushing these stubs around with a dielectric wand.

Microwave Power Measurements

The family of curves shown in Fig. 7 show power out vs. power in for as little as one unit connected into the circuit to as many as 6 units bonded into the circuit. It is evident that the gain is relatively independent of the number of units used. The output power increases monotonically with increased numbers of units, and the device behaves as a linear amplifier. The maximum output power attained was eight tenths of a watt at about 4 GHz, and under these conditions the rf voltage swing was of the order of 20 volts. Fig. 8 shows the result obtained for a single V gate transistor with a 14 mil source periphery. The amplifier was operated at 7 GHz and exhibited linear gain of 7 dB, saturated at 100 milliwatts output with 4 dB gain and a collector efficiency of 33%. The overall efficiency was 20 percent.

The power amplifier capabilities of GaAs MESFETS have just begun to emerge. It is the combined characteristics of high breakdown voltage associated with the Schottky-barrier electrode on GaAs together with the high saturation velocity of electrons in GaAs that make it well suited for a power amplifier at microwave frequencies.

Acknowledgements

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References

1. E. O. Johnson, "Physical Limitations on Frequency and Power Parameters of Transistors," RCA Review, pp. 163-177, June 1965.

2. O. Pitzalis, I. Martin, Private Communication.

3. C. A. Liechti, "GaAs Microwave Schottky-Gate FET," Digest ISSCC, Feb. 1972, Phila., Pa.

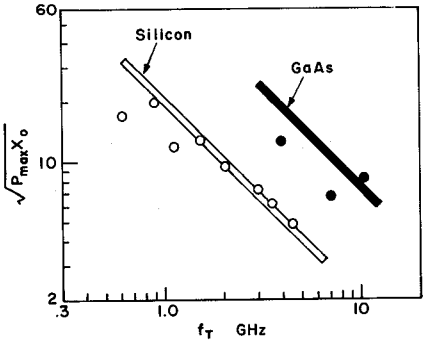


FIG. 1 POWER PER UNIT ADMITTANCE VS. f_t FOR SILICON AND GaAs TRANSISTORS

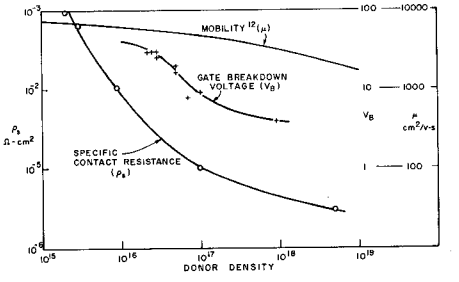


FIG. 2 MOBILITY, SPECIFIC CONTACT RESISTANCE, AND SCHOTTKY-BARRIER BREAKDOWN VOLTAGE VS. DENSITY FOR GaAs

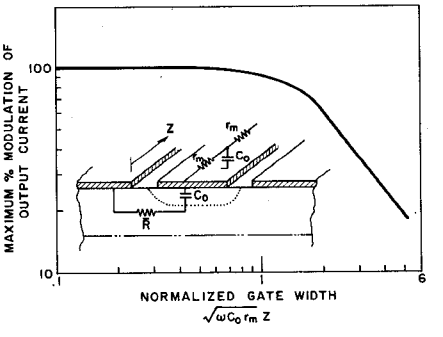


FIG. 3 PERCENTAGE OF MAXIMUM CHANNEL CURRENT MODULATION VS. NORMALIZED GATE WIDTH

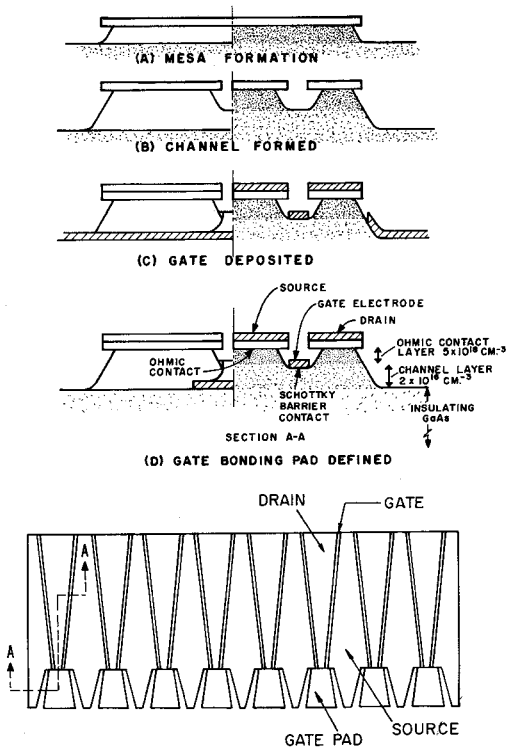


FIG. 4 PLAN VIEW AND CROSS SECTION OF MULTIGATE FET

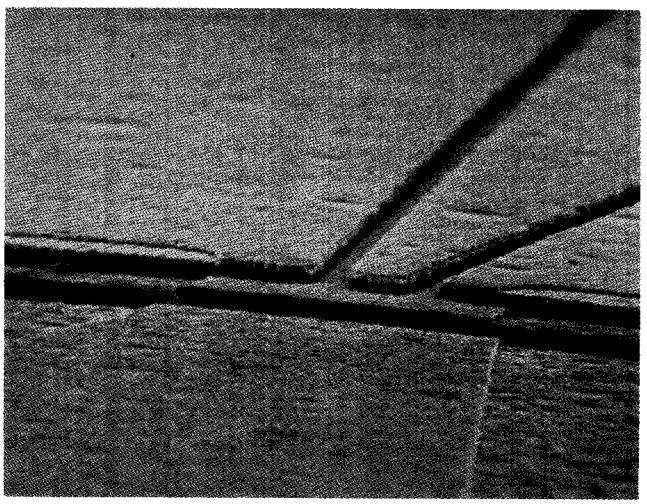


FIG. 5 SCANNING ELECTRON MICROGRAPH OF FET IN THE VICINITY OF A GATE BONDING PAD

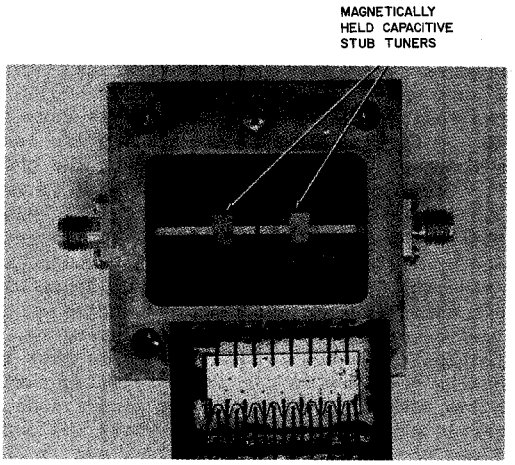
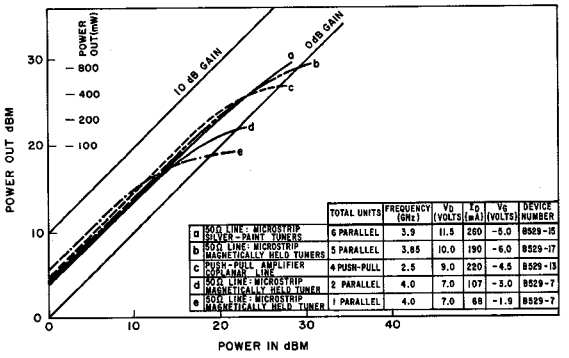


FIG. 6 PHOTOGRAPH OF FET IN MICROSTRIP TEST FIXTURE WITH INSET SHOWING CLOSEUP OF FET AND ASSOCIATED BONDING WIRES



		TOTAL UNITS	FREQUENCY (GHz)	V_D (VOLTS)	I_D (mA)	V_G (VOLTS)	DEVICE NUMBER
a	50Ω LINE: MICROSTRIP SILVER-PAINT TUNERS	6 PARALLEL	3.9	11.5	260	-5.0	B529-15
b	50Ω LINE: MICROSTRIP MAGNETICALLY HELD TUNERS	5 PARALLEL	3.85	10.0	190	-6.0	B529-17
c	PUSH-PULL AMPLIFIER COPLANAR LINE	4 PUSH-PULL	2.5	9.0	220	-4.5	B529-13
d	50Ω LINE: MICROSTRIP MAGNETICALLY HELD TUNER	2 PARALLEL	4.0	7.0	107	-3.0	B529-7
e	50Ω LINE: MICROSTRIP MAGNETICALLY HELD TUNER	1 PARALLEL	4.0	7.0	68	-1.9	B529-7

FIG. 7 POWER OUT VS. POWER IN FOR MULTIGATE FET

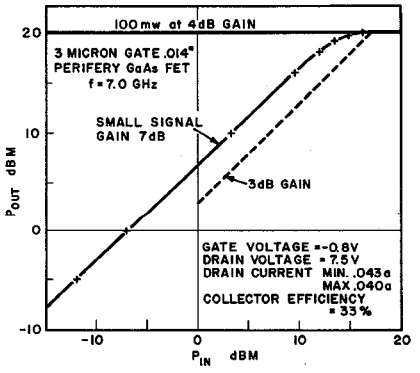


FIG. 8 POWER OUT VS. POWER IN FOR SINGLE GATE FET